CSC 362 Study Guide for Midterm 3
Exam Date: Wednesday, March 29 (tentative)

This examine covers material from Computer Organization and Architecture only.

Chapter 4: Know the role of and components of the CPU; know the fetch-execute cycle and the use of the various CPU registers. Know what the bus is, what is carried over each of the control, address and data bus, and the direction of communication from component to component over the three buses. Know how to interpret memory sizes (e.g., 4Gx32) as the number of addressable locations and word sizes, chip/bank organization, number of bits needed for an address, which bits are used to select the bank and address on the chip for low-order and high-order interleave. Know what interrupts are, why they are needed and steps are taken by the CPU whenever an interrupt arises. For MARIE, know the following: how the steps of the fetch-execute cycle are carried out, the use of these registers: AC, IR, PC, MAR, MBR, and the size of these components; be able to write RTN for instructions similar to the homework; be able to read and write MARIE code, and know how these operations function (what register movements are involved). You do not need to know the binary or hex op codes. Understand what consequence a change to MARIE might have on such things as the instruction length, size of memory and size of the registers as listed above.

Chapter 5: Know the issues for instruction formats: fixed vs. variable sized, number of operands, number of memory references per instruction, number and complexity of addressing modes, load-store instruction set, and how these decisions can impact the efficiency of a processor and a pipeline. You will not need to know the PDP-10, PDP-11, Intel or PowerPC formats but understand how they differ and the pros and cons that each instruction format provides. Given an instruction format, be able to determine the length of an instruction, or given an instruction’s length, be able to determine the size of addressable memory, immediate data and number of registers that can be addressed, etc. Know the addressing modes covered in the chapter and how each works. Given values stored in memory, be able to specify the datum stored in the AC for different addressing modes. Know what instruction-level pipelining is, how to compute the speedup of a pipeline over a non-pipelined processor, and how to compute speedup if there are data dependences or branches.

There will be no questions pertaining to Intel Assembly language on the exam.