CSC 362 Homework Assignment #4
Due Date: Monday, April 23

Word Processor all answers, show work for partial credit. Answer 10 of the 11 problems or all 11 for extra credit.

1) Identify the portions of the following code that support temporal locality of reference, spatial location of reference and sequential locality of reference.
   ```c
   for(i=0;i<n;i++)
   {
   a[i]+=c;
   if(a[i]%2==0)
   c++;
   }
   ```

2) Suppose a computer has 4 Gigabytes of memory and a cache of 256 blocks where each block can store 32 words. The word size is 64 bits and memory is word addressable.
   a. What is the format of memory addresses if the cache is direct-mapped?
   b. What is the format of memory addresses if the cache is 2-way set associative?
   c. What is the format of memory addresses if the cache is 8-way set associative?
   d. What is the format of memory addresses if the cache is fully associative?

3) Read problem #11 on page 393. Use the same memory and cache layout and determine for the 20 memory references below which ones are hits and which ones are misses, and compute the hit rate. Assume the cache is already loaded where block 0 has tag 2, block 1 has tag E, block 2 has tag 0 and block 3 has tag 2. The 20 memory references are: 0A, 0B, 0C, 0D, 03, 04, E7, E8, E9, 0F, 10, 11, 1F, 20, 21, EA, EB, EC, 13, 14. Since the references are in order, if there is a miss, you have to update the cache to keep track of what is currently stored. Your answer need only list whether each of the 20 accesses is a hit or miss (you don’t have to draw the cache as it updates). Also include the cache’s overall hit rate.

4) A computer uses an on-chip cache backed up by an off-chip cache backed up by main memory. Assume the on-chip cache has a hit time of .5 ns, the off-chip cache has a hit time of 3 ns and main memory has an access time of 12 ns. The on-chip cache has a hit rate of 91.1%, off-chip has a hit rate of 96.8% and main memory has a hit rate of 100%.
   a. What is the average memory access time for this machine?
   b. We want to add a second on-chip cache (the off-chip would be an L3 cache, the second on-chip would be an L2 cache). The L2 cache has a 1 ns hit time and 94.2% hit rate. What is the average memory access time now?
   c. Starting from part a (without the additional cache introduced in b), we add virtual memory with a TLB with a hit time of .5 ns hit time and hit rate of 99.3%, a page table in memory with the same hit time as main memory (12 ns) and a 100% hit rate, and a main memory hit rate of 99.9984% with the swapping process taking 500,000 ns. What is the average memory access time for this machine now?

5) What makes a set-associative or fully associative cache more expensive than a direct-mapped cache? What makes the direct-mapped cache have a poorer hit rate than any set-associative or fully associative cache? In spite of the poorer hit rate, we usually select a direct-mapped cache for our L1 cache and TLB. Why?

6) Assume a computer is word addressable with 256M of addresses and is running a process whose page table is given below. Answer the following questions.
   a. How big is a page/frame in words?
b. What is the physical address for the logical address 000011111111?

c. What is the physical address for the logical address 100010101010?

d. What is the physical address for the logical address 010101010101?

e. How large is this program (approximately) in words?

f. How much of the program is in memory?

<table>
<thead>
<tr>
<th>Page Number</th>
<th>Frame Number</th>
<th>Valid Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>22</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>----</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>23</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>----</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>----</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>94</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>----</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>12</td>
<td>1</td>
</tr>
</tbody>
</table>

7) We are considering making one of two adjustments to a pipelined processor. First, we might enlarge our TLB. The larger TLB will improve our hit rate by 15% over the current TLB and the TLB is 40 times faster than memory. Second, we might use a super pipeline in which our cache accesses are split into two stages. This allows us to double the speed of the system clock. This enhancement is used as often as there are no stalls. Assume that there is a 1 cycle stall on average for every 6 instructions. Use Amdahl’s Law to compute the overall speedups of both enhancements. Show the results.

8) What is the cost of moving from programmed I/O to interrupt-driven I/O? What is(are) the benefit(s)? What is the cost of moving from interrupt-driven I/O to DMA I/O? What is(are) the benefit(s)?

9) Examine the I/O controller on slide 12 of the chapter 7 power point notes and answer the following questions.
   a. The CPU communicates to the I/O controller over the ready or request line? The I/O controller communicates back to the CPU over the ready or request line?
   b. The authors label one line “Error”. What is this line used for and what should it be labeled?
   c. What does the address decoder do?

10) Imagine that we have 9 disks in a RAID 5 configuration where disk 9 stores a parity byte for the data bytes on the other 8 disks of the same location (track/sector/surface). If the 8 data bytes are as follows, determine the parity byte (assuming even parity): 00001111, 11111111, 10101010, 01010101, 11100111, 10111011, 00000011, 01000111.

11) Answer the following regarding the RAID levels:
   a. We use RAID 5 instead of RAID 4. In what way is RAID 5 better than RAID 4?
   b. A home computer users wishes to select some form of RAID for both improved storage access and some amount of redundancy but does not want a RAID 1 cabinet. Which would you recommend and why?
   c. Assume a RAID cabinet consists of 6 independent drives. Assume the same surface on the first and last drives both fail. Which RAID levels could potentially recover from the two failures? Explain.